

# DATA SHEET

**74F1240**

Octal inverter buffer (3-State)

Product specification  
Supersedes data of 1999 Jan 08  
IC15 Data Handbook

2000 Jun 30

## Octal inverter buffer (3-State)

74F1240

## FEATURES

- High impedance NPN base inputs for reduced loading (20 $\mu$ A in High and Low states)
- Low power, light loading
- Functional pin-for-pin equivalent of 74F240
- 1/30th the bus loading of 74F240
- Provides ideal interface and increase fan-out of MOS microprocessors
- Octal bus interface
- 3-State buffer outputs sink 64mA
- 15mA source current

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1240	3.5ns	40mA

## ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	DRAWING NUMBER
20-pin plastic DIP	N74F1240N	SOT146-1
20-pin plastic SOL	N74F1240D	SOT163-1

## DESCRIPTION

The 74F1240 is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables,  $\overline{OE}a$  and  $\overline{OE}b$ , each controlling four of the 3-State outputs.

## INPUT AND OUTPUT LOADING AND FAN OUT TABLE

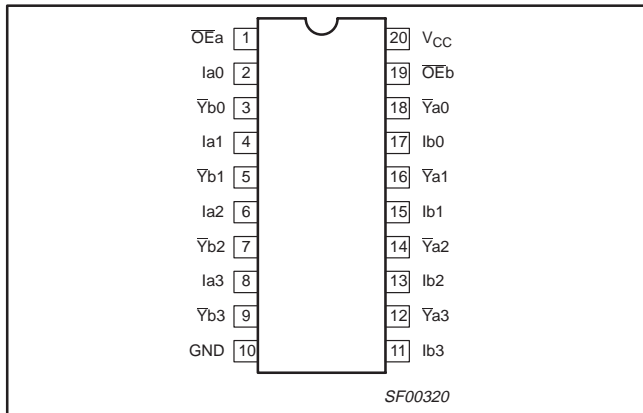
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs	1.0/0.033	20 $\mu$ A/20 $\mu$ A
$\overline{OE}a$ , $\overline{OE}b$	Output enable inputs (active Low)	1.0/0.033	20 $\mu$ A/20 $\mu$ A
$\overline{Y}an$ , $\overline{Y}bn$	Data outputs (74F1240)	750/106.7	15mA/64mA

**NOTE:** One (1.0) FAST unit load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

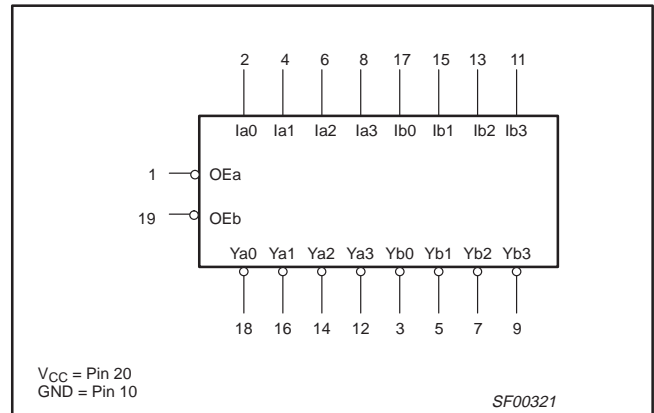
# Octal inverter buffer (3-State)

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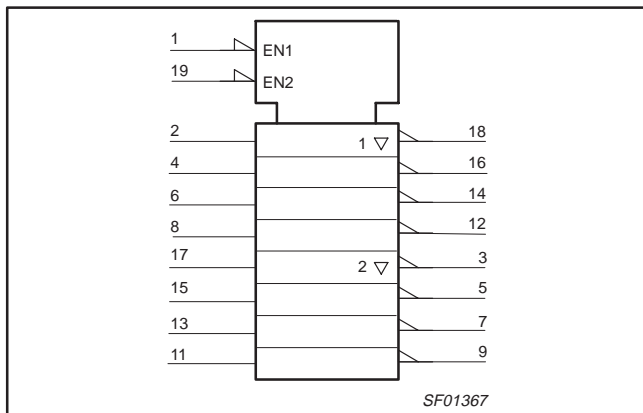
## PIN CONFIGURATION



## LOGIC SYMBOL



## IEC/IEEE SYMBOL

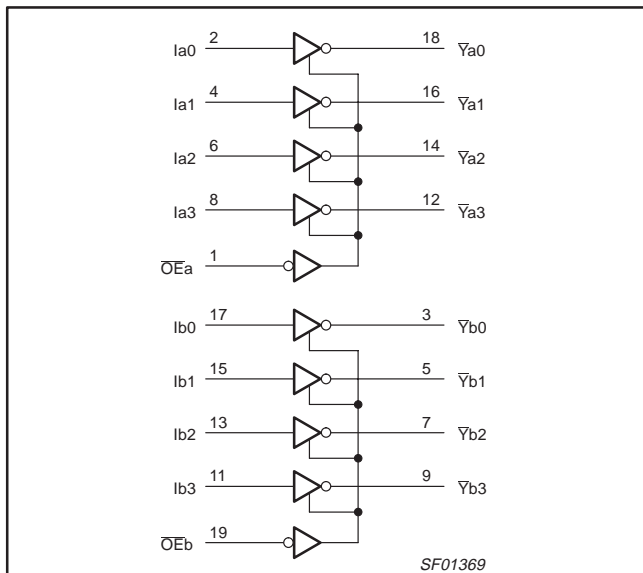


## FUNCTION TABLE

INPUTS				OUTPUTS	
OEa	Ia	OEb	Ib	Ya	Yb
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 Z = High impedance "off" state

## LOGIC DIAGRAM



## Octal inverter buffer (3-State)

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	128	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-15	mA
I <sub>OL</sub>	Low-level output current			64	mA
T <sub>amb</sub>	Operating free-air temperature range	0		+70	°C

## Octal inverter buffer (3-State)

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**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>			LIMITS			UNIT	
					MIN	TYP <sup>2</sup>	MAX		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN	I <sub>OH</sub> = -3mA	±10% V <sub>CC</sub>	2.4			V	
				±5% V <sub>CC</sub>	2.7	3.3		V	
			I <sub>OH</sub> = -15mA	±10% V <sub>CC</sub>	2.0			V	
				±5% V <sub>CC</sub>	2.0			V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN	I <sub>OL</sub> = 48mA	±10% V <sub>CC</sub>		0.38	0.55	V	
			I <sub>OL</sub> = 64mA	±5% V <sub>CC</sub>		0.42	0.55	V	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>				-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = 0.0V, V <sub>I</sub> = 7.0V					100	μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V					20	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V					-20	μA	
I <sub>OZH</sub>	Off-state output current, High-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V					50	μA	
I <sub>OZL</sub>	Off-state output current, Low-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V					-50	μA	
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX			-100		-225	mA	
I <sub>CC</sub>	Supply current (total)	I <sub>CCH</sub>	V <sub>CC</sub> = MAX				22	30	mA
		I <sub>CCL</sub>					58	75	mA
		I <sub>CCZ</sub>					44	58	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

**AC ELECTRICAL CHARACTERISTICS**

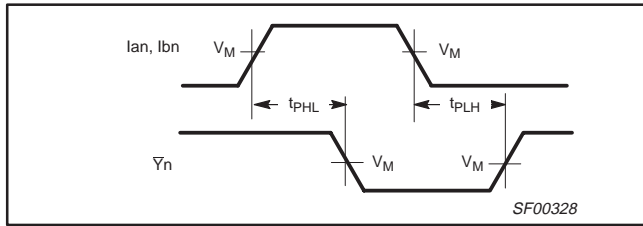
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay I <sub>an</sub> , I <sub>bn</sub> , to $\bar{Y}_n$	Waveform 1	3.0 1.5	4.5 2.5	6.5 4.5	2.5 1.5	7.5 5.0	ns ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time to High or Low level	Waveform 3 Waveform 4	3.0 4.0	5.5 7.0	7.5 9.0	3.0 4.0	8.0 9.5	ns ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time to High or Low level	Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 5.5	2.0 2.0	6.5 6.0	ns ns

# Octal inverter buffer (3-State)

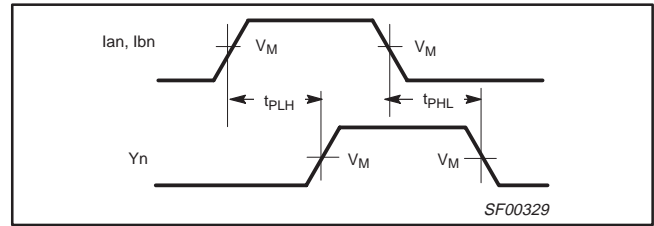
74F1240

## AC WAVEFORMS

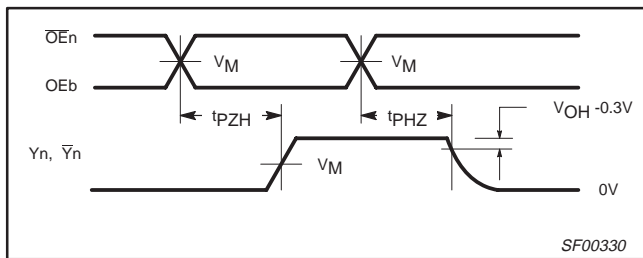
For all waveforms,  $V_M = 1.5V$ .



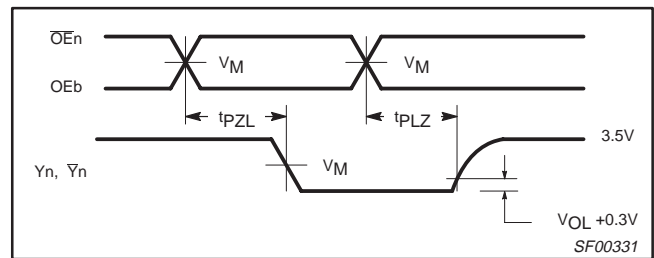
Waveform 1. For Inverting Outputs



Waveform 2. For Non-inverting Outputs



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

## TEST CIRCUIT AND WAVEFORMS

**Test Circuit for Open Collector Outputs**

**Input Pulse Definition**

**SWITCH POSITION**

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

**DEFINITIONS:**

$R_L$  = Load resistor; see AC electrical characteristics for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

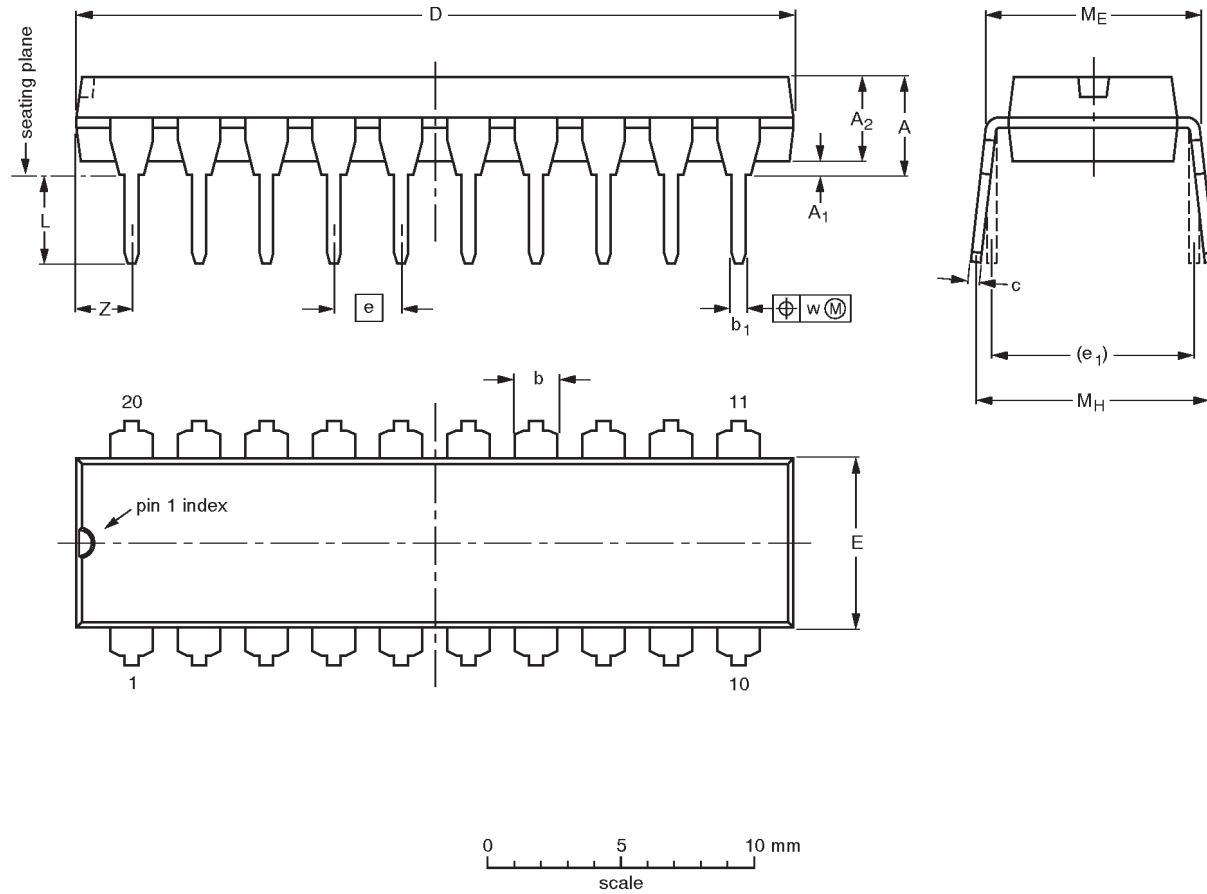
SF00128

# Octal inverter buffer (3-State)

74F1240

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

# Octal inverter buffer (3-State)

74F1240

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	$\theta$
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT163-1	075E04	MS-013AC			95-01-24 97-05-22



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**NOTES**

## Octal inverter buffer (3-State)

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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